

ABSTRACT OF THE DISCLOSURE

A data input circuit converts input serial data to n-bit parallel data, and outputs the n-bit parallel data by following an address signal. The data input circuit includes a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to the data shifting unit through the input column. Thus, the data input device can speed up its processing speed with a simplified circuit structure whose circuit size is reduced.

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